Name:-Suhas Madhukar Kolse

Roll No.:-E43039

VHDL Code:-library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_3039 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end HA\_3039;

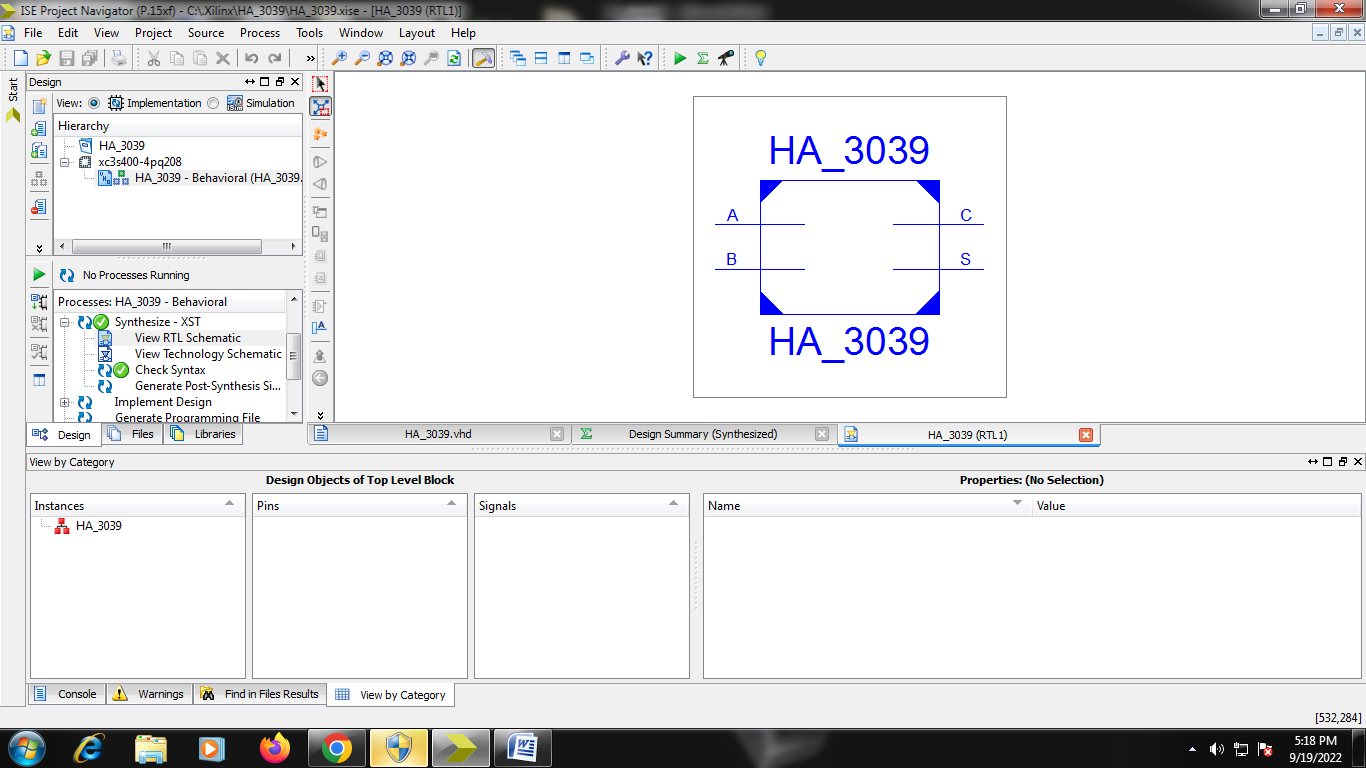
architecture Behavioral of HA\_3039 is

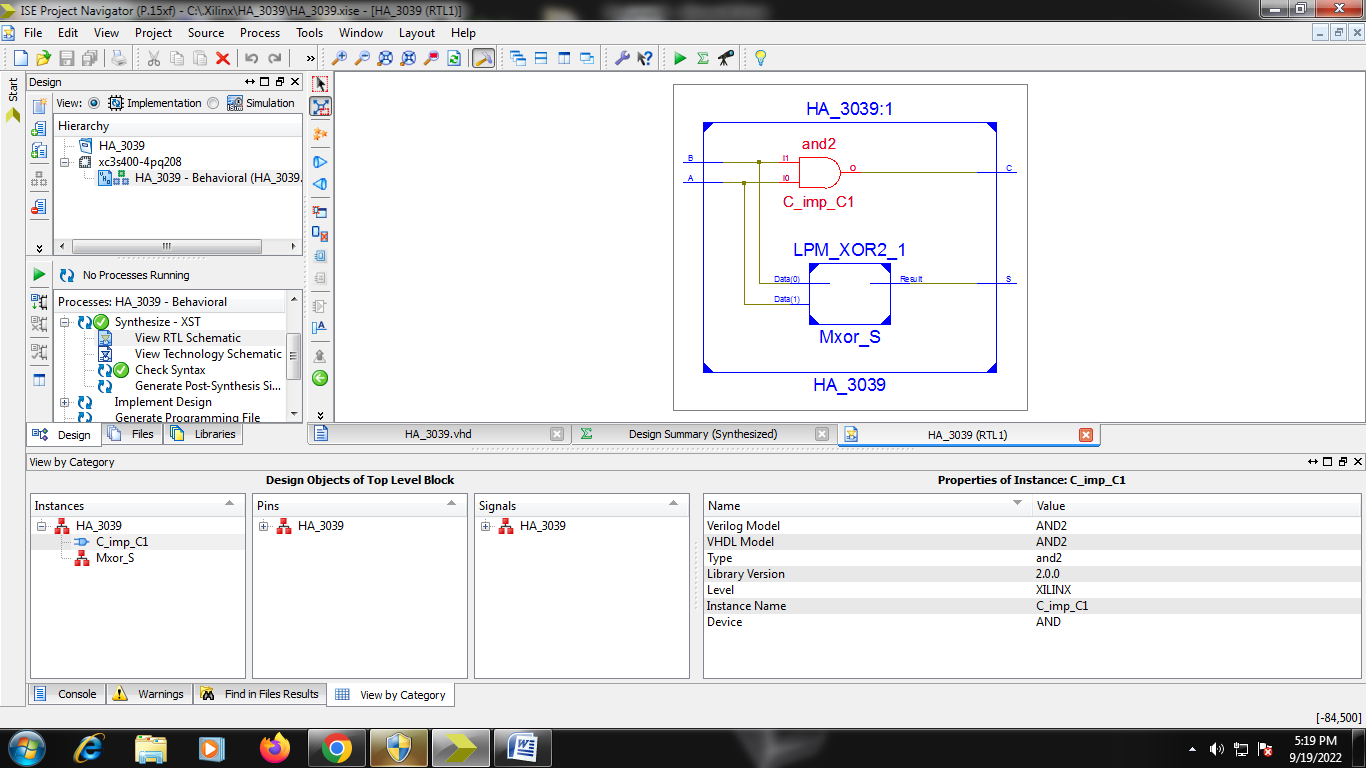
begin

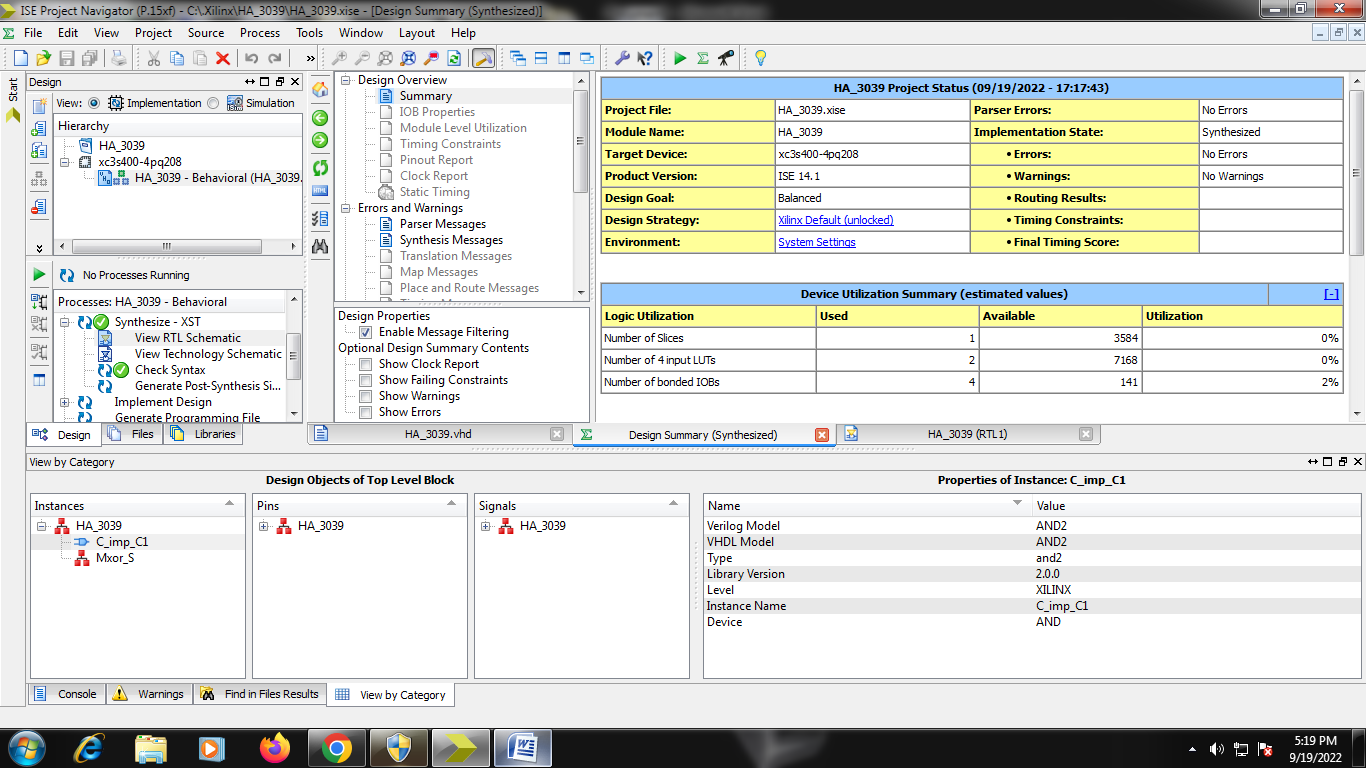
S<= A XOR B;

C<=A AND B;

end Behavioral;

RTL Schematic:-



Design Summary:- 

Test\_bench:- LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY HA\_TB\_3039 IS

END HA\_TB\_3039;

ARCHITECTURE behavior OF HA\_TB\_3039 IS

COMPONENT HA\_3039

PORT(

A : IN std\_logic;

B : IN std\_logic;

S : OUT std\_logic;

C : OUT std\_logic

);

END COMPONENT;

--Inputs

signal A : std\_logic := '0';

signal B : std\_logic := '0';

--Outputs

signal S : std\_logic;

signal C : std\_logic;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: HA\_3039 PORT MAP (

A => A,

B => B,

S => S,

C => C

);

-- Stimulus process

stim\_proc: process

begin

A<='0';

B<='0';

Wait for 100 ns;

A<='0';

B<='1';

Wait for 100 ns;

A<='1';

B<='0';

Wait for 100 ns;

A<='1';

B<='1';

Wait for 100 ns ;

-- hold reset state for 100 ns.

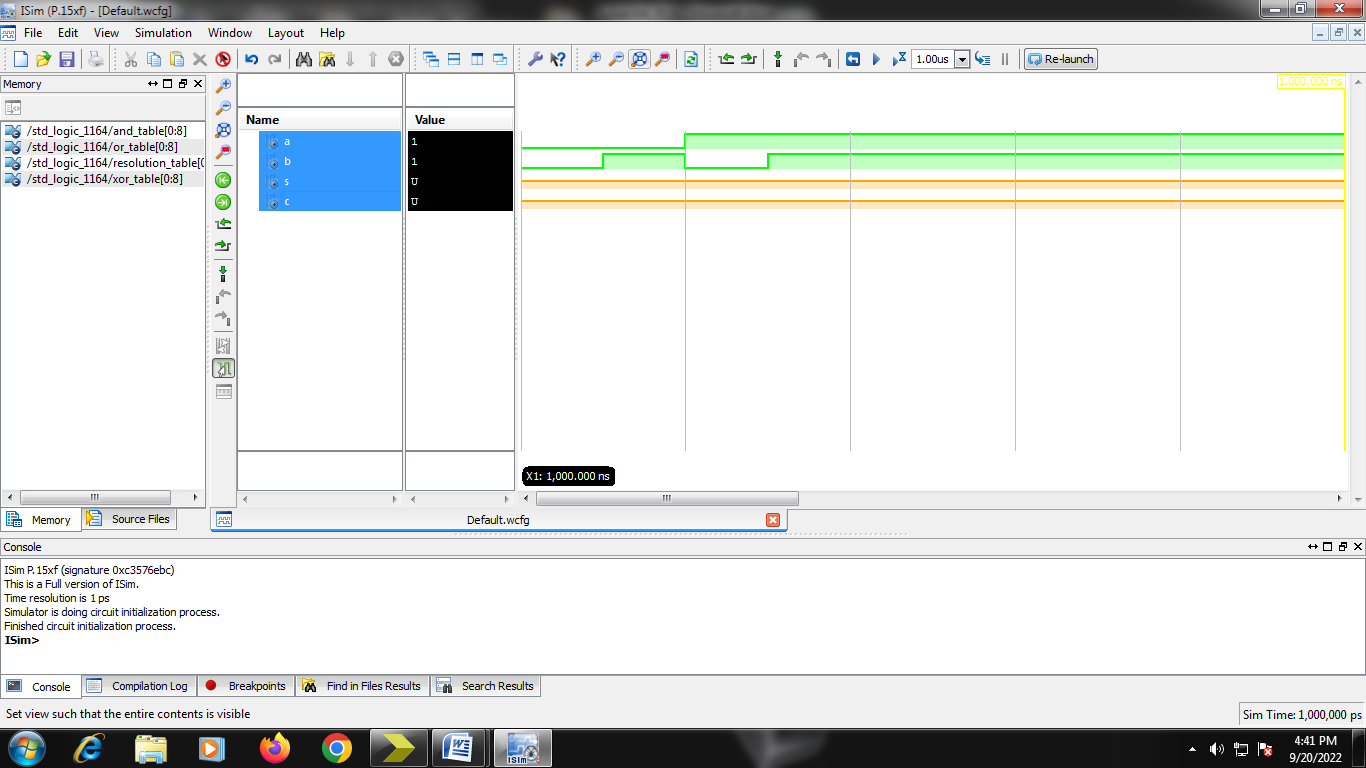
wait for 100 ns;

-- insert stimulus here

wait;

end process;

END;

Waveform:=

=========================================================================

\* Final Report \*

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Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.033ns

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Process "Synthesize - XST" completed successfully